VIDEOGRAPHIC SYSTEM ARCHITECTURE DESCRIPTION

The Videographic system is designed around eight dynamic RAMs, which are available from many sources at very low cost. The system timing was designed to operate with the slowest (lowest cost) dynamic RAMs available in the industry. This insures compatibility with all parts from all credible vendors. Among the parts which can be used are the MOSTEK MK4096-15 (a very low cost high-threshhold fallout part), any other part in the MK4096 family (all other parts are faster than the "-15"), and any MK4027 part by any credible vendor. The 4027 is a newer design for the 4096 bit dynamic RAM, and is presently manufactured by all major semiconductor manufacturers.

The price for the 4K dynamic RAM is already low (example: $1.86 for 100K pieces over one year for the MK4096-15); and it is likely that the price will improve through 1978. The main reason for this expectation is the emergence of the 16K RAM as the current wonder of the semiconductor world. Just as the 4K RAM caused its predecessor, the 1K RAM to decline in price, it is reasonable to expect the influence of the 16K RAM to do the same to the 4K pricing.

The parameter which most strongly affects 4K RAM pricing, namely access time, has been accounted for in the system such that any part with a 350 nanosecond access time or faster will work in the design. For a point of reference, the slowest MK4027 made by MOSTEK is the MK4027-4 at 250 nanoseconds, and the slowest part from Texas Instruments is the TMS 4027-25 at 250 nanoseconds.

The use of dynamic RAM insures the lowest cost per bit achievable in semiconductor RAM technology. The dynamic RAM will always be less expensive than its static RAM counterpart. This is because the dynamic RAM chip is inherently smaller than the static RAM chip for the same density.

The most unique design achievment of the Videographic system is the manner in which a single bank of 4K x 8 dynamic RAMS (8 chips) serve three system functions:

1. Video Refresh Memory (1K)

2. Character Memory (2K)

3. System Scratchpad (1K)

This means that the maximum capability system requires no additional RAM beyond the eight 4K RAMs in the video section.

The 1K x 8 Video Refresh Memory stores character information on a matrix of 32 columns by 28 rows. This character information can be written as well as read by the CPU using any of the CPU memory reference instructions. The "memory mapped" interface technique is used, in which every screen location corresponds to a unique CPU memory address. The "read-back" feature of this memory makes software efficiencies possible, since characters in the refresh memory (which are visible on the TV screen) can be read directly off the screen, with no additional software overhead required to keep track of all images and positions. This is especially useful in detecting coincidence between images.

The 2K x 8 Character Memory stores the bit patterns which control the appearance of the dot patterns which appear on the screen. Each character is defined as a matrix of dots 8 across and 8 high. Each character code in the refresh memory "looks up" eight 8-bit bytes in the character memory to generate the dot pattern for the character code. The eight bit code in character memory is capable of accessing 2^8 or 256 different characters. Since each character occupies 8 bytes of data, the character memory size for 256 characters is 256 x 8 or 2048 (2K) bytes.

The refresh/character memory combination allows 256 software-defined characters to be created at one time. Since the character memory is treated as system read-write memory, the image dot patterns can be revised by the CPU at any time in a game program. This allows an unlimited image repertoire so long as the limitation of 256 characters concurrently on the screen is recognized.

The remaining 1K x 8 of RAM is used as system scratchpad. It is in this memory that the Z80 stack is stored, as well as general purpose read-write memory need by system software.

The access time to the video screen is an important parameter, especially when large, complex images must be moved. The system architecture allows virtually instantaneous access to the entire 4K video memory. Specifically, the system adds a maximum of one microsecond to the execution time of any memory reference instruction which accesses the video memory system.

Color is implemented in a memory-efficient manner. A small (8 word x 8) memory stores color information. This memory can be ROM or PROM for fixed color schemes, or RAM for software loadable color schemes. The 8 x 8 RAM is implemented in the System Control Chip.

Colors are defined in image/background pairs. The 256 possible character codes are divided into eight groups of 32 characters each. Each of these groups can be assigned an independent image/background color pair. It is possible to create images which are identical except for color, by simply putting the same image code into two different character memory locations (thereby assigning two different character codes to the same image). The color encoding is done using four bits, which allow a repertoire of sixteen possible colors.

Figure One is a diagramatical rendering of the basic five-chip system. The five chips consist of two standard parts (the Z-80 and the I/O chip) and three custom chips (the Video Interface Chip, VIC; The Timing Generator, and the System Control Chip).

The Z-80 is chosen for the microprocessor chip mainly because of its interfacing simplicity and powerful instruction set. Many of the instructions which were added to the Z-80 to enhance the 8080 instruction set are well suited to performing graphics. Two examples of this graphic instruction efficiency are the Rotate Memory instruction, which allows dots to be moved without first loading them into the Accumulator; and the Memory Move instruction, which allows large blocks of memory to be moved with very few instructions.

The Z-80 should be in plentiful supply, especially in the time frame beginning with first quarter 1978. MOSTEK and ZILOG are now in full production, with commitments to two large volume customers: Bally and Radio Shack.

The I/O chip is a standard Z-80 system component (ZILOG Z80-PIO; MOSTEK MK3881). Sixteen I/O lines which can be individually designated input or output by the CPU are provided, along with interfacing circuitry which allows integration into a Z-80 system with no external circuitry.

The Video Interface Chip contains video synchronization circuits to develop the sync and blanking signals for the video monitor; a multiplexor to control the CPU/video interaction and develop address inputs for the system RAM; and video outputs (composite sync, composite blanking, video). This chip replaces approximately 20 TTL packages. The video signals developed by this chip are all TTL level outputs. These outputs may be combined in various manners to provide black and white or color capability.

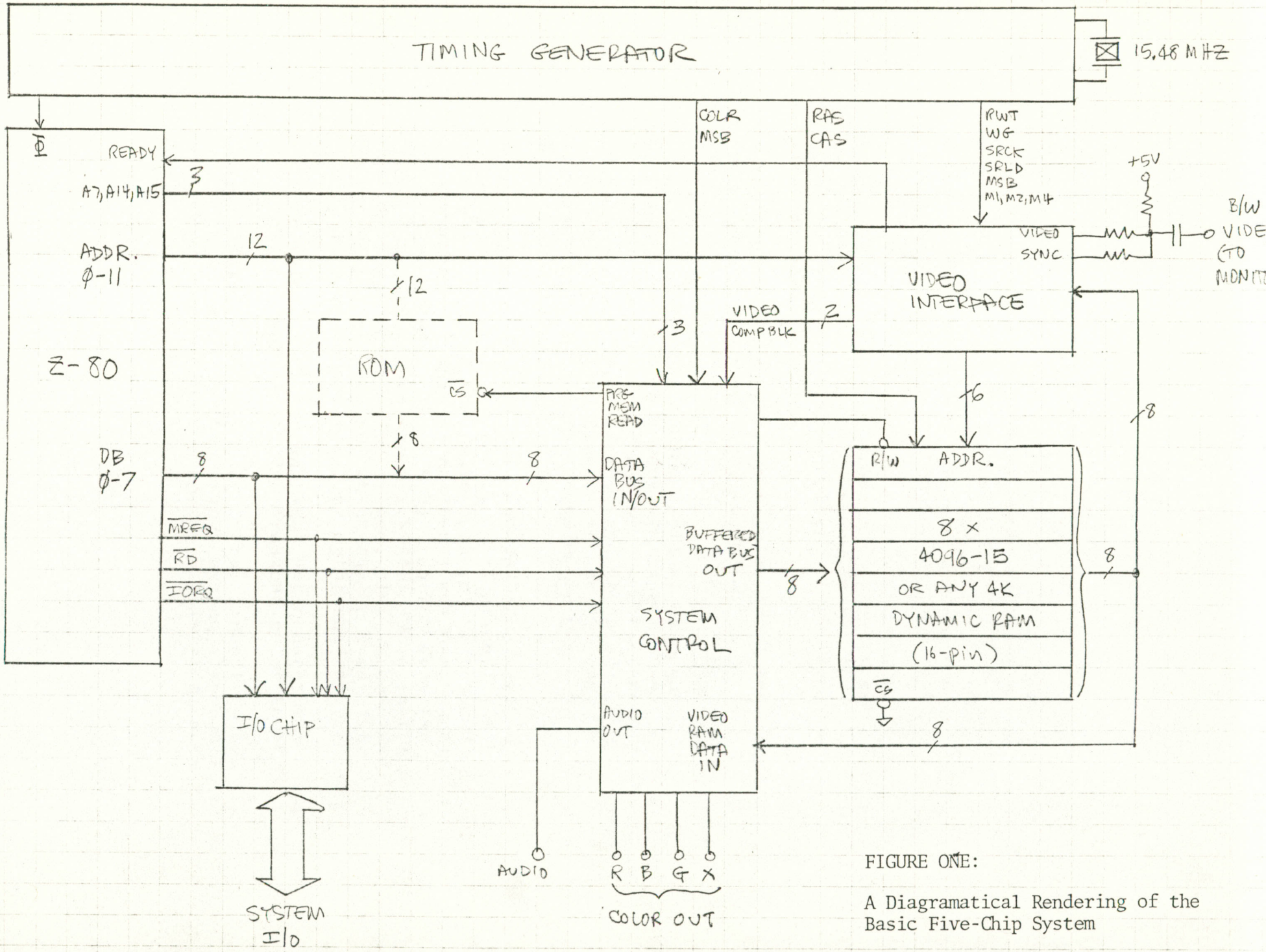

FIGURE ONE:

A Diagramatical Rendering of the Basic Five-Chip System

The VIC is implemented using bipolar technology. This technology was dictated mainly by the SRCK (shift register clock) signal, which makes a transition every 192 nanoseconds. A secondary consideration was the multiplexor control signals, which, although not as fast as the SRCK signal, require several gate levels of decoding. The VIC contains buffers on all I/O pins so that a minimum system may be constructed without any additional buffer circuits.

The Timing Generator Chip develops all of the system timing signals. Due to the high clock frequency (15.48 MHz), this chip also requires bipolar technology. This chip replaces approximately six TTL chips.

The System Control Chip provides many assorted functions to the chip set. As presently defined, it contains the following circuitry:

1. Bus control. The eight bidirectional data bus lines from the CPU are split into a separate input and output bus. The output lines from the RAM system are connected to the System Control Chip, buffered, and gated onto the bidirectional bus at the appropriate times. The output bus, which does not leave the chip, is fed to the color encoding circuitry, and the tone generator.

2. Color Encoder. The color is encoded as described in the Architecture section of this specification. The highest frequency signal in the System Control Chip occurs in this section (VIDEO). This signal has a maximum transition time of 192 nanoseconds. The CPU has control over the color scheme by writing into the 8 x 8 RAM. Note that there are four TTL-level color outputs--Red, Blue, Green, and "X". The "X" output is a spare, which may be used either to provide 16 different colors, or color shading.

3. Tone generator. This is an eight bit counter which can be set to one of approximate 200 frequencies by the CPU.

4. System Control. Address and control lines from the CPU are decoded and routed to the various system components (program memory ROM, video RAM, I/O ports). This eliminates external system decoding circuitry.

Pricing

Following is budgetary pricing information on the Videographic chip set.

1.	Z-80 Microprocessor	$ 7.00	Note 1
2.	Z-80 I/O chip (e.g. MK3881)	$ 4.00	Note 1
3.	Video Interface Chip	$ 5.00	Note 2
4.	Timing Generator Chip	$ 4.60	Note 3
5.	System Interface Chip	$ 4.30	Note 4
6.	8 ea. 4K Dynamic RAMs @ $1.80	$14.40	Note 5
	TOTAL	$39.30	

Note 1. Per a telephone conversation with Bob Schweitzer (Manager, Microprocessor Marketing of MOSTEK) 6 September 1977. These estimates are for 200 - 300 thousand over a one year period starting first quarter 1978. Both prices are "first cut", with considerable moving room (especially in a MOSTEK package including RAMs). A price of $8.00 for the pair, especially for the latter part of 1978 should not be unreasonable.

Note 2. This chip has been designed, and will be in production starting October 1977. Gremlin Industries uses this chip in all video game products. Price quoted is for 200,000 pieces during 1977-78. Vendor is Silicon Systems, Inc.

Note 3. Estimated by Silicon Systems, Inc. Bipolar IC, 18-pin package. Development cost is $40,000., with first articles estimated at 26 weeks after start.

Note 4. Estimated by Silicon Systems, Inc. Quoted for 200,000 quantity over one year. Assumes that the chip design is achievable in MOS. 40-pin plastic package. Development cost is $40,000., first articles estimated at 26 weeks after start.

Note 5. Assumes a "relaxed-spec" dynamic RAM, available from many sources. As explained in the specification, the system is designed to take advantage of these low cost parts.

There is room for improvement in this price, since the quantity for 200,000 systems would be 1.6 million RAMs. The $1.80 figure is based on a current price for 0.1 million RAMs.

NOT INCLUDED IN THIS QUOTATION

The following items, which are necessary for a consumer videographic computer are not included in this quote:

1. Color encoder. This circuit translates the four TTL-level color outputs from the system control chip to a phase-modulated "color burst" signal suitable for consumer color TV sets.

2. Video Combination Circuit. This circuit combines the video, color burst, and sync signals into a composite signal compatible with a color TV.

3. RF modulator. This circuit, which requires FCC type-approval, uses the composite video signal to modulate an RF carrier, so that the video signal may be connected directly to the antenna terminals of the TV set, and in effect be "broadcast" into the color TV set. Associated with this circuit is an antenna switch which must provide the FCC-required isolation between the video game output, the Television antenna, and the Television.

4. Power supply, enclosure, ROMs, controls.

NOTE: Items 1 - 3 might be combined into a single chip.

Implementation Alternatives

The chip set described in this specification is not the only possible mechanization of the Videographic system. It is probable that the system cost could be significantly reduced by redefining the chip set with the cooperation of a MOS manufacturer. This could produce a chip set which is optimized to the manufacturer's processes, and thus would likely be more efficient and lower cost. Also, definitive specifications which are unique to Milton Bradley's plans could be incorporated into the architecture.