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PRELIMINARY

TARGET SPECIFICATION

INTELLIVISION III

	WRITTEN	APPROVED		
BY				

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Target Specification for Intellivision III Feature List

Objectives:

- 16 Colors - 4/Card
- 8 Moving Objects/Line Up to 16 Pixels Wide in 2 Colors or 8 Pixels Wide in 4 Colors
- Reversible Objects (Goal)
- 20 X 24 Cards (Graphics) 40 X 24 (Goal)
- 40 X 24 Alphanumerics
- Frame Pointer
- Resolution 320 X 192 or Better Than Intellivision (Background & Moving Objects)
- External Video Overlay Capability — Intellivision format only
- 2 X CPU
- Color to Change at Field Rate (line rate as goal)
- Sound Chip on CPU (future) SOUND/IO
- More Freq Range on Sound TBD
- Voice Capability
- RHC Receiver Decoder on CPU — goal
- Compatibility to "Old Cartridges
- System Upgradable

Scope

This document describes a second generation architecture for Intellivision III. The design has been created to provide a significant upgrade to the STIC I system (4x) while closely focusing on the requirement of direct compatibility with game cartridges written to operate on the earlier system.

The text provides an overview of the system structure and connectivity of the integrated circuits. The individual devices are also described including the performance details designed into this system.

System Overview

To support the enhanced graphics requirements which require a minimum of two times the bus bandwidth of STIC I it becomes necessary to employ a different system architecture. Additional to a new architecture the demand for a more graphic data manipulation forces the additional need for at least a two times increase in instruction throughput for the CPU.

The wider bus bandwidth and the need to support a faster CPU places the constraints of faster memory throughout the system.

To achieve the above and make use of standard RAMs wherever possible, it becomes necessary to develop a system bus structure that will enable the graphics device and the CPU to coprocess with the same memory space with each being transparent to the other.

To enable the system to have uniformity in its bus structure, all devices, i.e., ROM, RAM, I/O, Graphics, CPU, shall utilize identical control signals, and address schemes.

Uniformity is achieved by employing the standard multiplexed address and control used by todays dynamic RAMs.

Supporting first generation cartridges is achieved by using the 16 bit wide data bus at both address and data.

System Description

The system is composed of three major functional blocks, namely a CP1610-2 microprocessor, a STIC 1B graphics support processor and system memory. The architecture has been optimized to permit transparent coprocessing operation of the system memory while providing a very high video data bandwidth. To support this architecture the CPU bus utilization cycles are carefully interleaved with the synchronous operation of the video chip.

The system clock operates at 3.56 and all bus operations are related to an eight cycle sequence which corresponds to eight screen pixels drawn per 2.2useconds. Within these eight cycles the CPU uses a pair of cycles to access the 16 bit memory bus every 2.2usec. During the horizontal retrace period of active picture the CPU is disabled. During all other periods the CPU is active. The remaining six cycles from the octet are used in a variety of modes to support the graphics image. The modes are listed in Table.

The connectivity of the system shall be based upon a single 16 bit bus and a separate multiplexed address bus. The 3.5 MHz clock provides a 14 Onsec half cycle period and memory access cycles are controlled by 28 Onsec RAS and CAS period. The memory map consists of a single continuous 65K word memory space. This simplicity allows any memory configuration of ROM or RAM to be used

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directly for graphic character storage and large ROMs may be considered as basic silicon video disks. The complete address space is always available to the processor and any desired change of color, object pattern, position etc., may be performed via software at any time.

The system has been designed to support two distinct operating configurations an enhanced multiple color, reusable object mode and a simpler STIC I (Intellivision III) cartridge compatible mode.

Enhanced Mode

The IB system makes very efficient use of dynamic memory structures and adopts a paging implementation whenever possible. This technique, for example, permits the 32 words of foreground object descriptions to be accessed in only 34 system cycles compared to the 64 required by alternative architectures. To complement the efficiency of dynamic RAMs it is proposed to construct a 16 bit wide ROM Design which uses a RAS, CAS multiplexed address configuration identical to the RAM area.

The bus configuration of the 1B enhanced mode is shown in Figure 1

Intellivision III Compatible Mode

The provision of compatibility is achieved through the addition of hardware on both the CPU and graphics chip which allows these devices to modify their architecture and bus cycle sequences to accept program code from a current 10 bit ROM cartridge.

The operational characteristics and memory map of the system shall be compatible with an Intellivision 1 implementation, but the detail system timing and logic implementation beyond the cartridge compatibility is significantly different.

The bus configuration in STIC I compatible mode is shown in Figure 2

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Circuit Descriptions

CP1610-2

The CP1610-2 is a 16 bit microprocessor designed as a performance upgrade on the earlier CP1610 series device. This circuit operates in a dual mode configuration where one mode provides bus compatibility with 10 bit cartridge ROMs designed to operate with a CP1610. In the compatible mode, the device supports a multiplexed data/address bus and validates its control sequence on three pins labelled BC1, BC2, BDIR.

This new CPU contains specific memory map logic which recognizes the memory configuration of an Intellivision III system and adjusts its instruction timing to emulate that system at the cartridge port.

In the upgraded mode, the CP1610-2 operates with a two times speed increase and significantly modified bus sequences. The device automatically re-configures to support a separate data and address bus, where the address is itself multiplexed in the RAS, CAS configuration of industry standard dynamic RAMS.

The CP1610-2 contains interrupt, DMA and auto refresh circuitry designed to support the STIC 1B system and to emulate the real time constraints of an Intellivision 1 unit.

In addition to its function as a microprocessor, the CP1610-2 also contains a 5 channel audio output similar to the 8914 sound chip used in the Intellivision 1 and a Remote Hand Controller Decode circuitry.

STIC 1B

The STIC 1B device is a logical extension of STIC I and STIC IA as used in the Intellivision I master component. This new device provides several performance enhancements while retaining the basic architecture of a multiple plane, background/foreground philosophy.

Similar to other circuits in this second generation design the STICK IB chip is a dual mode device which contains specific hardware to support emulation of Intellivision I system graphics. While providing a exact emulation capability, the detailed logic implementation and bus sequences are considerably modified in this implementation.

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System ROM

This second generation graphics system is highly optimized on bus utilization and general architecture. To maintain the system throughput requires a different philosophy of ROM design. The required change organizes the ROM architecture to operate similar to a section of standard dynamic RAM. That is, the data bus is maintained separate to a multiplexed address bus, and two control/clock signals are used to access the appropriate memory location whithin the chip , namely row address select RAS, and column address select CAS.

The timing of these signals operate on a 280 nanosecond cycle and the expected read access time of the ROM should be 460 nanoseconds for the first RAS, CAS sequence and 180 nanoseconds for each subsequent CAS cycle within same row address.

The ROM device must contain its own memory map circuitry operating from both the multiplexed address bus and the two wire chip enable code which is valid during the RAS, CAS cycle.

The memory organization is structured on a 16 bit parallel word with a 8K X 16, thus providing words in the initial version of the device.

Section A

Should a RAS/CAS ROM be not available for production start-up, the addition of a latch will allow use of OFF the same ROMS as a back-up position.

RAM Requirement

This system has been designed to operate with industry standard dynamic RAMs. A 16 bit parallel data bus is employed and several device configurations are possible. Acceptable system operation can be achieved using 4K words of memory and this complement would be best achieved by using four of 16K X 8 RAMs. As the system is extended through full bit map support, presentation level protocols and personal computer applications it is anticipated that more memory would be added up to a full complement of 65K words.

The system operates under a seven bit multiplexed address bus but an 8/6 combination could be implemented if memory cost makes that the best alternative. The RAS, CAS cycles operate on a 280 nanosecond cycle and memory supporting an access time of roughly 460 nanoseconds is required.

Manual Interface

The exact connection for hand controllers has not been completed. It is assumed that a remote control configuration will be used with communication performed over a serial bus.

Section B

To allow for manual hand controller input a TTL multiplexer with minor decoding logic will allow game play for remote hand controller override.

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Background Detail

The basic display format shall support 24 rows of 20 cards (40 cards goal) with each card being defined as a matrix of 16 X 8 pixels. To permit fine scroll at the pixel definition, the architecture shall fetch 25 rows of 41 cards to provide the fractional edge cards that occur during most offset values. The combination of cards and pixel matrix amounts to a total visible resolution of 320 horizontal by 192 vertical. The pixel rate shall be synchronized to the chroma clock and the non interlace mode will normally be used for a game only display with interlace being reserved for configurations where the chip is operating sync and phase locked to an external video source.

The display logic, actually supports each row of cards independently and in full operational mode several control parameters must be passed to the row display logic. These parameters include the descriptor list start address, the desired X and Y offset, the display operating mode and any color pallette changes.

The color pallettes are areas of RAM comprising sixteen, twelve bit words. The desired pallette for each card is selected by a three bit field within each descriptor. The twelve bit color select code provides four bits for each of red, blue and green control, thus supporting 4096 actual color values.

The object pattern array may be positioned anywhere in the memory address space of 65K words including the cartridge ROM or expansion RAM space.

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Foreground Detail

The specific support of each foreground object shall be based upon a descriptor and control array contained in general system memory, a video pattern store integrated into the video-chip and the standard object pattern array implementation as shared with the background display logic. The descriptor and control array shall comprise four 16 bit words which define position, orientation, priority, interaction history and object pattern array address.

The object pattern for foreground objects will be preaccessed by the video chip during the horizontal retrace period. Up to TBD words of object pattern may be fetched for each object and depending upon color mode, a foreground object may be either TBD or TBD pixels wide. The vertical height is controlled by a simple counter and may extend for 255 lines.

The foreground object logic is automatically reusable with the video chip simply accessing the next individual object descriptor and control array in sequence. If all ogjects were minimum height, i.e., one line, each of the eight objects could be reused 192 times. The reuse feature interrupts the processor at each activation and records on internal storage the current status of the object stack. The foreground objects may be randomly used in either color mode either color mode either in a line or over the complete frame.

The object array patterns are accessed by a double indirect sequence using two pointers. The initial memory address and object position shall be defined through the descriptor and control array which describe a rectangular area where the object may exist. The second pointer offers a relative offset of how the object pattern may be displayed within this rectangle.

The interaction of foreground objects is supported by two different techniques. The Intellivision I compatible structure uses object overlap as defined within STIC I documentation. The upgrade to this approach supports interaction through an overlap detect of individual color selections as defined by the object array patterns. This approach offers the important improvement of defining selective areas of an object as being interactive, (such as the feet of a player) where the rest of the image is used to enhance the graphical effect. The use of an indirect pointer means that the area defined as interactive may be created in a color identical to the noninteractive image if desired.

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Electrical Characteristics

These characteristics apply to all LSI devices which are specifically designed to operate in a STIC IB system and include the CP1610-2, the graphics chip and the program ROMS.

Absolute Maximum Ratings

Temperature Under Bias	$0^{o}C$ to + $100^{o}C$
Storage Temperature	- $55^{o}C$ to +$150^{o}C$
All Input or Output Voltages with respect to VSS	- 0.2V to +7.0V
VCC with respect to VSS	- 0.2V to +7.0V

Operational Specification

Ambient Temperature	$0^{o}C$ to +$70^{o}C$
Supply Voltage	VCC = +4.75V -+5.25V
	VSS = 0. 0V

Characteristic

Inputs	Sym	Min	Max	Units	Conditions
Input Logic Low	VIL	0	0.7	Volts	
Input Logic High	VIH	2.2	VCC	Volts	
Input Leakage	IIL		5	uA	VIN = 0V to VCC
Capacitance	IIC		10	pf	VIN = 0V at 1MHz
Outputs					
Output Logic Low	VOL	0	0.5	Volts	IOL = 1.3mA +150pf
Output Logic High	VOH	2.4	VCC	Volts	IOH = 12QuA
Supply Current					
VCC Supply	ICC		100	mA	